source region **12** and an N+ drain region **17** at the top surface. The source region **12** electrically connects to a source electrode **S** at the bottom surface of the semiconductor die **11.** A P+ region **14** provides a conductive path to the N+ source region **12.** A metal portion **18** shorts out a p+ body region **19** and the N+ source region **12** to provide an electrical path between the source region **12** to the source electrode **S.** A drain electrode **D** and a gate **G** are also at the top surface of the semiconductor die **11.** For clarity of illustration, the gate oxide corresponding to the gate **G** is not shown in FIG. 1. The source electrode **S** at bottom surface of semiconductor die **11** is attached to a metallic substrate **13.** The metallic substrate **13** serves as both a heat sink and a ground reference for the source electrode **S.** Wires (not shown) are coupled to the gate electrode **G** and the drain electrode **D** to provide the semiconductor die **11** with input and output connections. In operation, source current flows from the metallic substrate **13,** laterally through the drift region **16** to the drain region **17,** and out of the semiconductor die **11** to a wire (not shown) coupled to the drain electrode **D.**--

Please replace the paragraph at page 2, line 12 with the following paragraph:

--**[08]** One embodiment of the invention is directed to a semiconductor die package comprising: a semiconductor die comprising a vertical power transistor, wherein the semiconductor die has a first surface and a second surface; a source region at the first surface of the semiconductor die; a gate at the first surface of the semiconductor die; a drain region at the second surface of the semiconductor die; a ground plane proximate the second surface and distal to the first surface; and a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the source region of the semiconductor die to the ground plane.--

Please replace the paragraph beginning at page 3, line 1 with the following paragraph:

--[10] Another embodiment of the invention is directed to a semiconductor die package comprising: a semiconductor die comprising a vertical power transistor, wherein the semiconductor die has a first surface and a second surface; an emitter region at the first surface of the semiconductor die; a base region at the first surface of the semiconductor die; a collector region at the second surface of the semiconductor die; a ground plane proximate the second surface and distal to the first surface; and a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the emitter region of the semiconductor die to the ground plane.--

Please replace the paragraph beginning at page 3, line 9 with the following paragraph:

--[11] Another embodiment of the invention is directed to a semiconductor die package comprising: a semiconductor die comprising a transistor, wherein the semiconductor die has a first surface and a second surface; a source region in the semiconductor die; a gate in the semiconductor die; a drain region in the semiconductor die; a ground plane proximate the second surface and distal to the first surface; and a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the source region of the semiconductor die to the ground plane.--

Please replace the paragraph beginning at page 3, line 27 with the following paragraph:

--[16] FIG. 4 shows a top view of a portion of a semiconductor package according to an embodiment of the invention.--

Please replace the paragraph beginning at page 6, line 10 with the following paragraph:

--[32] The bus members according to embodiments of the invention can have flat portions that form angles. For instance, the bus member **26** shown in FIG. 2 has a horizontal portion coupled to the source region **126** of the semiconductor die **30** and at least one leg that extends downward toward the ground plane **20**. Preferably, the bus member **26** has two (or more) legs that extend to the ground plane **20** at opposite ends of the semiconductor die **30**. The bus member **26** electrically couples the ground plane **20** to the source region **126**. One leg is shown by the dotted lines in FIG. 2. In some embodiments, the horizontal portion of the bus member **26** can be a continuous body of metal and can cover a major portion of the first surface **31(a)** of the semiconductor die **30** (e.g., greater than 50% of the area of the first surface **31(a)**). Solder in the form of hemispherically shaped logs, balls, columns, etc. can be used to electrically couple the horizontal portion of the bus member **26** to various source region connections at the first surface **31(a)** of the semiconductor die **30**. Solder can also be used to couple the ends of the one or more legs of the bus member **26** to the ground plane **20**.--

Please replace the paragraph beginning at page 7, line 12 with the following paragraph:

--[36] FIG. 4 shows a top plan view a portion a semiconductor die package with the inner leg surface of the bus member **26** shown by dotted lines. As shown in FIG. 4, the horizontal portion **26(a)** can cover a majority of the upper surface of the semiconductor die **30**. An area **30(b)** of the semiconductor die **30** under the horizontal portion **26(a)** of the bus member **26** can include source regions. An exposed